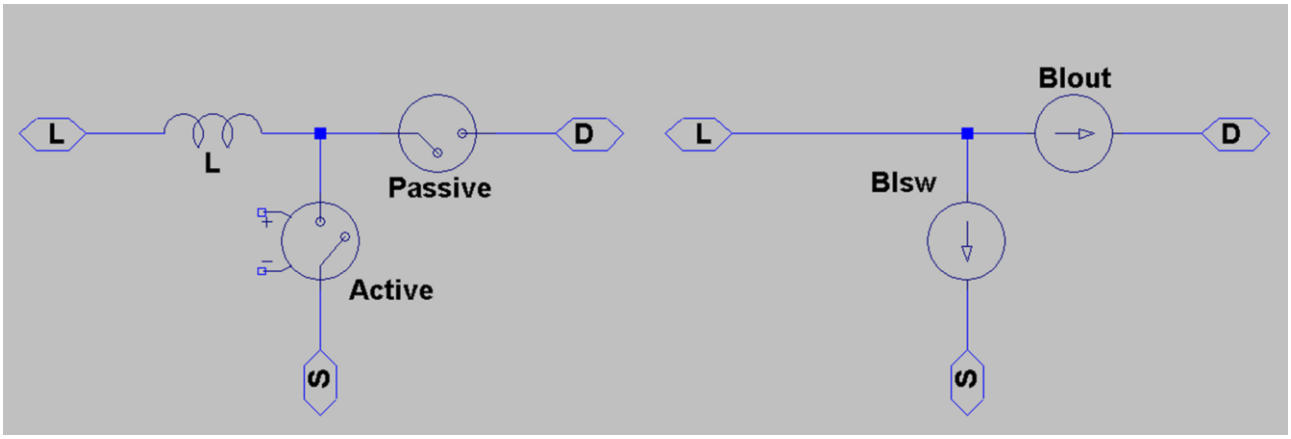
Introduction

Simulations involving power converters can be increased in speed significantly when done with average switch models. The possibility to study the switching behavior itself is lost but the behavior of control loop and the response on input and output variations is reproduced accurately.
In many applications DC to DC converters are operated in the critical (border) mode. Linear critical mode average switch models are available for LTSpice as CM_1v0.
When the exact current shapes or the power losses within the average switch are of specific interest then a linear model won't suffice. In this release a non-linear critical mode average switch model CM_NL_0v9 is presented. It simulates the three most important non-linear effects of a critical mode switch accurately. Compared to the linear model some simulation speed is lost but compared to a HF simulation the non-linear average model is still much faster.

Model description

The average switch replaces the main components of the power stage of a DC-DC converter: the active switch, the inductor and the passive switch by a set of controllable current sources. The way the replacements are carried out to get from the HF to the AVerage model is shown in the figures below.



HF model AV model

Up, Down and Flyback converters can all be constructed with the same diagrams. Only the meaning of the three terminals differs across the topologies. The following table shows those differences.

Topology↓ Terminal→	L	S	D
UP	Input	Common	Output
DOWN	Output	Input	Common
FLYBACK	Common	Input	Output

Table1: topologies.

Because of the mathematical analogy between the Up, Down and Flyback topologies the same equations can be used for the behavioral sources BIsw and BIout in all three cases. Formally it also suffices to use only one

symbol for the topologies but then a complication arises with the passive switch terminal **D**. Since the passive switch can only conduct current in one direction it would make a difference if the input voltage of the converter is positive or negative. This is not a favorable property of the model since it would require a parameter to set the correct passive switch direction. To circumvent this complication the orientation of the passive switch has been made visible in the symbol.

Technical details

Topologies and operating ranges

A straightforward DC to DC critical mode average converter model only requires the desired peak coil current as an electrical quantity. In the symbol this is a fourth terminal called *Ipk*. The value of the peak current is accepted as a voltage on this pin. It must always be positive or zero.

A minimum voltage between the pins D,L and between L,S is maintained by the subcircuit and can be specified with a parameter *Vmin*.

Converter	Polarity in	Passive switch	CM_NL Model	Operating range
Down	Positive	inward	cm_nla	Vin>Vout+Vmin; Vout>Vmin
	Negative	outward	cm_nlk	Vin<Vout−Vmin; Vout<−Vmin
Up	Positive	outward	cm_nlk	Vout>Vin+Vmin; Vin>Vmin
	Negative	inward	cm_nla	Vout<Vin−Vmin; Vin<−Vmin
Flyback	Positive	inward	cm_nla	Vin>Vmin; Vout<−Vmin
	Negative	outward	cm_nlk	Vin<−Vmin; Vout>Vmin

Table2: model characteristics.

Current sense delay

Current sense delay is the first non-linear effect. It is the time needed for the current sensor, the control IC, the driver and the switch to turn off the switch current after the peak current set point *Ipk* has been reached. The value *Tcs* must be specified on a Value line of the symbol.

Zero crossing detection delay

Zero crossing detection delay is the second non-linear effect. It is the time needed for the zero crossing detector, the control IC, the driver and the switch to turn on the switch current after coil current has reached zero. The value *Tzcd* must be specified on a Value line of the symbol.

Parallel capacitance

Parallel capacitance is the third non-linear effect. It is the total capacitance across the switch and consists of parasitic switch capacitance and pcb, wiring and housing capacitances. Parasitic capacitance can be non-linear so an effective value over the applied voltage range has to be used. The value *Cp* must be specified on a Value line of the symbol.

Coil inductance

The non-linear effects all depend on the inductance of the converter coil. The value *L* must be specified on a Value line of the symbol.

Minimum current set point

A practical converter will not draw any current if the peak current set point is too close to zero. In the cm_nl models a threshold is defined below which the switch will stop working. This is the threshold current *Ithr*.

Internal time constant
The subcircuit uses several A-devices and B-sources. The rise time of the A-devices and the time constant formed by the output resistance of the B-devices and their parallel capacitors can be chosen by parameter *timeC*. It is recommended to experiment with the value and find a compromise between speed and accuracy. Values in the order of 1% of the smallest HF switching period will generally work fine.

Parallel capacitance
The subcircuit has parallel capacitors for the two current sources BIsw and BIout. They have the value *parC* that can be specified on a Value line of the symbol.

Minimum and maximum frequency
The subcircuit uses the resulting switching frequency internally to calculate currents. Since divisions by the frequency are necessary it is necessary to set a minimum positive value *Fmin* on a Value line of the symbol. A value just below the lowest HF frequency will suffice. Optionally a maximum limit to the frequency can be set with parameter *Fmax*. A value e.g. twice the highest HF frequency will do.

Minimum voltage
Voltages between pins L, S and D must be within the operating ranges for a valid result. If they are not the model will clamp them to the operating ranges in order to remain stable. The subcircuit also uses equations in which the voltages between the pins L, S and D appear in the denominators of divisions. These are the reasons for having the parameter *Vmin* that can be specified on a Value line of the symbol. It sets the value of the internal clamps. This proved to be the implementation that results in the highest simulation speed while maintaining a reasonable reliability in case of fault conditions. Note that in extreme circumstances the clamps won't work. They have an internal resistance of 1mΩ and a forward drop of 1mV. As a consequence the voltages can still reach zero if currents in the order of 1kA are passed through the clamps.

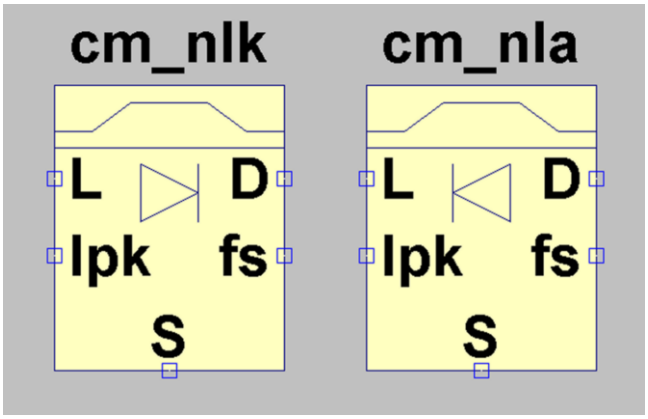
Parameter list
The following parameters can be specified on the SpiceLine of the symbol:

Name	Description	Default	Unit	Limits
Cp	Switch (parasitic) parallel capacitance	1p	F	>0
Fmin	Minimum frequency in internal formulae	1	Hz	>0
Fmax	Maximum frequency in internal formulae	1G	Hz	>Fmin
Ithr	Threshold for current set point	1µ	A	>=0
L	Converter coil inductance	1m	H	>0
parC	Parallel capacitance between L,S and L,D	1p	F	>0
Tcs	Current sense delay	1n	s	>=0
timeC	Internal time constant	1n	s	>0
Tzcd	Zero crossing detection delay	1n	s	>=0
Vmin*	Minimum voltage between L,S and D,L	100m	V	>0

* Note: a positive value is required for both cm_nlk and cm_nla.

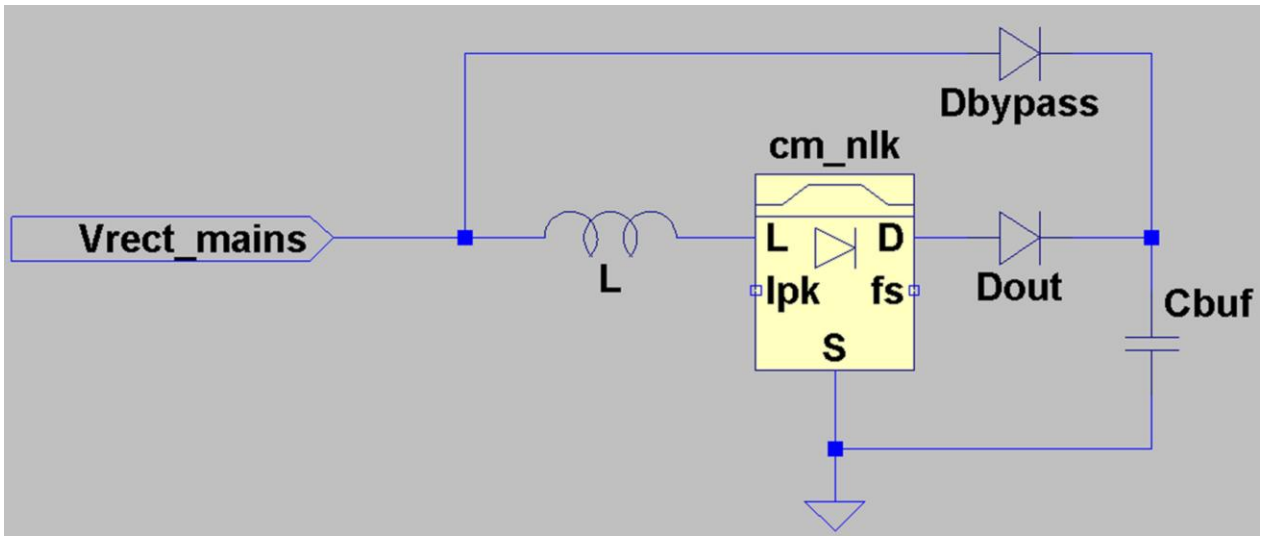
Symbols

The symbols for CM_NL_0v9 are shown at the right. The **cma_nl** (pin D = anode) model and the **cmk_nl** (pin D = cathode) model differ in the forward direction of the passive switch.



Properties & Application notes

- The models use LTSpice A-devices.
- The voltage applied at the Ipk pin is referred to Gnd and connected to it by a 1GΩ resistor.
- No current may be drawn from the **fs** pin.
- During the inrush phase of a converter the average switch is operated outside the operating area but the model attempts to keep the pin voltages within the operating range. In the practical circuit there may also be a bypass diode for the inrush phase. It is recommended to connect an up converter-PFC model as follows:



Rectified mains has a bypass diode directly to the output buffer capacitor. The model is connected by means of the components an HF model would have had: the converter coil L and the output diode Dout. By choosing the *Vmin* parameter well below the forward voltage of the diodes (but above zero) a realistic current distribution over the Dout and Dbypass paths is obtained.

- It is recommended to set LTSpice's maximum time step. In contradiction to what one would expect the model often simulates faster when the time step is limited.